ABSTRACT OF THE DISCLOSURE

A semiconductor chip package includes a ground metal layer disposed in close proximity to a signal layer for carrying electrical input and output signals to and from the chip. The ground metal layer has a plate structure and is formed by two metal plates or a single metal plate having openings for the electrode pads of the chip. Because the ground trace is nearest to the signal trace, the loop area formed by a signal current and its return current is reduced and, therefore, loop inductance is reduced as well. Further, because of the plate structure of the ground trace and its proximity to the signal trace, the inductive element and parasitic parameters due to the signal trace can be significantly reduced and the electrical performance of high-frequency semiconductor IC devices is greatly improved, especially when applied to wafer level packaging IC devices.